PATENT
Attorney Docket No. 97703

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No. 7,080,195

Confirmation No. 6808

Issued: July 18, 2006

Name of Patentee: Ngai et al.

Patent Title: MERGING INDICATIONS OF MATCHING ITEMS OF MULTIPLE GROUPS AND POSSIBLY ASSOCIATED WITH SKIP CONDITIONS TO IDENTIFY WINNING ENTRIES OF PARTICULAR USE FOR IMPLEMENTING ACCESS CONTROL LISTS

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service on the date shown with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on September 4, 2006.

9-4-2006
Kirk D. Williams, Esq.

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR PATENT OFFICE MISTAKE (37 C.F.R. § 1.322)

Attn: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

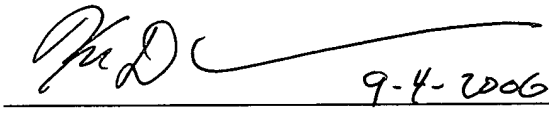
It is requested that a Certificate of Correction be issued to correct Office mistakes found the above-identified patent. Attached hereto is a Certificate of Correction which indicates the requested correction. For your convenience, also attached are copies of selected pages from (a) the issued patent with errors highlighted, and (b) Amendment A filed January 16, 2006, with the correct text/instructions.

In re US Patent No. 7,080,195

It is believed that there is no charge for this request because applicant or applicants were not responsible for such error, as will be apparent upon a comparison of the issued patent with the application as filed or amended. However, the Assistant Commissioner is hereby authorized to charge any fee that may be required to Deposit Account No. 501430.

Respectfully submitted,
The Law Office of Kirk D. Williams

Date: September 4, 2006

By  9-4-2006

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,080,195

DATED : July 18, 2006

INVENTOR(S) : Ngai et al.

It is certified that error(s) appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 5, line 10, replace "value, etc." with -- value, etc. --

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PATENT NO. 7,080,195
No. of additional copies

⇨ NONE (0)

SEP 13 2006

data to facilitate interpreting the data or performing operations on it, such as, but not limited to memory locations or devices, sets, queues, trees, heaps, lists, linked lists, arrays, tables, pointers, etc. A data structure is typically maintained in a storage mechanism. The terms "pointer" and "link" are used generically herein to identify some mechanism for referencing or identifying another element, component, or other entity, and these may include, but are not limited to a reference to a memory or other storage mechanism or location therein, an index in a data structure, a value. etc. The term "associative memory" is an extensible term, and refers to all types of known or future developed associative memories, including, but not limited to binary and ternary content addressable memories, hash tables, TRIE and other data structures, etc. Additionally, the term "associative memory unit" may include, but is not limited to one or more associative memory devices or parts thereof, including, but not limited to regions, segments, banks, pages, blocks, sets of entries, etc.

The term "one embodiment" is used herein to reference a particular embodiment, wherein each reference to "one embodiment" may refer to a different embodiment, and the use of the term repeatedly herein in describing associated features, elements and/or limitations does not establish a cumulative set of associated features, elements and/or limitations that each and every embodiment must include, although an embodiment typically may include all these features, elements and/or limitations. In addition, the phrase "means for xxx" typically includes computer-readable medium containing computer-executable instructions for performing xxx.

In addition, the terms "first," "second," etc. are typically used herein to denote different units (e.g., a first element, a second element). The use of these terms herein does not necessarily connote an ordering such as one unit or event occurring or coming before another, but rather provides a mechanism to distinguish between particular units. Additionally, the use of a singular tense of a noun is non-limiting, with its use typically including one or more of the particular thing rather than just one (e.g., the use of the word "memory" typically refers to one or more memories without having to specify "memory or memories," or "one or more memories" or "at least one memory", etc.). Moreover, the phrases "based on x" and "in response to x" are used to indicate a minimum set of items x from which something is derived or caused, wherein "x" is extensible and does not necessarily describe a complete list of items on which the operation is performed, etc. Additionally, the phrase "coupled to" is used to indicate some level of direct or indirect connection between two elements or devices, with the coupling device or devices modifying or not modifying the coupled signal or communicated information. The term "subset" is used to indicate a group of all or less than all of the elements of a set. The term "subtree" is used to indicate all or less than all of a tree. Moreover, the term "or" is used herein to identify a selection of one or more, including all, of the conjunctive items.

Disclosed are, inter alia, methods, apparatus, data structures, computer-readable medium, mechanisms, and means for merging indications of matching items of multiple groups and possibly associated with skip conditions to identify winning entries of particular use for implementing access control lists. In one embodiment, indications are received from an associative memory bank indicating which locations were matched during a lookup operation. Each of the entries is typically associated with one or more hierarchical groups and a skip or no-skip condition. The matching entries are merged to identify one or more wining entries, these being matching entries not in a group that is skipped. A group is typically skipped if the highest priority matching entry of the particular group is associated with a skip condition. A priority encoder can be used to identify a single highest priority winning entry from the winning entries.

One embodiment includes an associative memory bank which generates matching indication signals for each matching entry that matches a lookup value. A merging mechanism is used to identifying a winning entry or multiple winning entries, if any, from the entries identified as matching. Each of the associative memory entries is associated with one or more hierarchical groups and a skip or a no-skip condition. The merging mechanism selects a winning entry based on the matching indication signals from the associative memory. This selecting typically includes identifying as a winning entry an entry first in the priority ordering of the entries that is not in a group that is skipped, wherein a particular group is skipped if the highest priority matching entry of the particular group is associated with a skip condition.

One embodiment includes one or more banks of one or more storage elements for identifying for each entry: (a) the associated skip or no-skip condition, and (b) whether or not said particular entry is first in the order sequence of one of the ordered plurality of groups. In one embodiment, each group corresponds to a different access control list. In one embodiment, the merging mechanism includes circuitry for identifying and masking skipped entries of the matching entries.

FIG. **1A** is a block diagram illustrating a system used in one embodiment for merging indications of matching items of multiple groups and possibly associated with skip conditions to identify winning entries. Associative memory entries **100** typically correspond to two or more groups of entries, and each entry is typically associated with a skip/no-skip condition. As shown, entries **100** correspond to multiple access control lists **103** (e.g., first-level groups of entries) and also different features **105** (e.g., second-level groups of entries). These associations are provided to merging mechanism **108** as indicated by configuration information **106** (e.g., storage devices, received signals, etc.). Associative memory entries **100** are matched against a lookup value and generates match/no-match indications **107**. These are typically parallel signals (e.g., one high or low signal for each entry indicating a match or no match), but may be any signaling or communications mechanism. Merging mechanism **108** identifies one or more winning entries **109** based on match/no-match indications **107** and configuration information **106**. In one embodiment, merging mechanism **108** includes a priority encoder or other mechanism to identify a single, highest-priority winning entry **109**.

In one embodiment, merging mechanism **108** identifies as the winning entry a matching entry first in the priority ordering of the entries that is not in a group that is skipped, wherein a particular group is skipped if the highest priority matching entry of the particular group is associated with a skip condition. In one embodiment, merging mechanism **108** identifies as the winning entry an entry first in the priority ordering that is not in one of the hierarchical groups that is skipped. One embodiment supports two levels of hierarchical groups; while one embodiment supports more than two levels of hierarchical groups with the exact number of levels being determined typically based on the needs of a particular application using an embodiment.

FIG. **1B** is a flow diagram illustrating a process for identifying a winning entry used in one embodiment. Pro-

Filed: Amendment A - Filed January 6, 2006

Amendments to the Specification:

Please replace the paragraph beginning on page 8, line 13, with the following amended paragraph:

The term "storage mechanism" includes any type of memory, storage device or other mechanism for maintaining instructions or data in any format. "Computer-readable medium" is an extensible term including any memory, storage device, and/or storage mechanism. ~~, and other storage and signaling mechanisms including interfaces and devices such as network interface cards and buffers therein, as well as any communications devices and signals received and transmitted, and other current and evolving technologies that a computerized system can interpret, receive, and/or transmit.~~ The term "memory" includes any random access memory (RAM), read only memory (ROM), flash memory, integrated circuits, and/or other memory components or elements. The term "storage device" includes any solid state storage media, disk drives, diskettes, networked services, tape drives, and other storage devices. Memories and storage devices may store computer-executable instructions to be executed by a processing element and/or control logic, and data which is manipulated by a processing element and/or control logic. The term "data structure" is an extensible term referring to any data element, variable, data structure, database, and/or one or more organizational schemes that can be applied to data to facilitate interpreting the data or performing operations on it, such as, but not limited to memory locations or devices, sets, queues, trees, heaps, lists, linked lists, arrays, tables, pointers, etc. A data structure is typically maintained in a storage mechanism. The terms "pointer" and "link" are used generically herein to identify some mechanism for referencing or identifying another element, component, or other entity, and these may include, but are not limited to a reference to a memory or other storage mechanism or location therein, an index in a data structure, a value, etc. The term "associative memory" is an extensible term, and refers to all types of known or future developed associative memories, including, but not limited to binary and ternary content addressable memories, hash tables, TRIE and other data structures, etc. Additionally, the term "associative memory unit" may include, but is not limited to one or more associative memory devices or parts thereof, including, but not limited to regions, segments, banks, pages, blocks, sets of entries, etc.

Col 5, line 10